SSD92-M-0019

NASA MSFC/ROCKWELL SSD

VERICODE AUTOMATIC IDENTIFICATION SYSTEM (VERISYSTEM) EVALUATION SUMMARY REPORT

Contract NAS8-38550
WBS 1.2.1.2.D

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Rockwell International

Space Systems Division
Huntsville Operations

SUMMARY

On May, 20, 1991 Rockwell International Corporation, Space Systems Division (SSD), Huntsville Operations, initiated a detailed evaluation of the Veritec, Inc., Vericode Automatic Identification System, known as the Verisystem. The system evaluation, performed for the NASA Marshall Space Flight Center (MSFC), ran for 130 working days and was completed on November 22, 1991. The Verisystem was selected for testing by NASA because of its unique capability to generate variable sized machine readable symbols which can be readily applied to hardware.

The Verisystem tests were structured to validate supplier claims and to define (bracket) upper and lower limits of system operation. Once these limits were defined, they were compared against limits that would be encountered during actual shuttle program use, and the results were recorded. The report is divided into four major sections that focus on label generation, stencil generation, hardware marking, and symbol decoding tests. Test results are summarized in a condensed system specification included and identified as Appendix B.

After an extensive review of system capabilities, the test team concluded that the Verisystem concept is sound and has reached a point in its development where limited application outside the laboratory is not only feasible but recommended. A list of proposed follow-on development tasks and future system implementation activities have been provided in the report.

Three hardware items, currently under development, are necessary before the Verisystem can be implemented on a programwide basis. The three are: the interface mechanism required to link the Verisystem transparently with the user's host computer; a versatile scanner lens that can view a larger range of symbol sizes; and a series of portable, handheld scanners needed to support manufacturing, test, and operations functions. No major technical problems have been identified that constrain development of these items.

Our in-depth review of possible system applications and benefits concluded that the Verisystem, if implemented on current or future programs, will contribute to improved operations and cost efficiency.

CONTENTS

CONTENTS

ILLUSTRATIONS

TABLES

APPENDICES

1.0 INTRODUCTION

This report summarizes the results of evaluation tests performed on the Veritec, Inc., Vericode Automatic Identification System (United States patent number 4,924,078). The Verisystem test program was conducted by Rockwell International Corporation, Space Systems Division (SSD), Huntsville Operations, in response to a task assignment from NASA, Marshall Space Flight Center (Contract NAS8-38550, Modification 6).

2.0 PURPOSE

The purpose of the evaluation test program was to identify the strengths and/or weaknesses of the Vericode Symbol and related system hardware as they apply to the marking of Space Shuttle Orbiter, Shuttle-C, and National Launch System (NLS) hardware, software, and documentation. The evaluation included the identification of possible Space Shuttle Program applications and estimated cost savings.

Tests were not performed to evaluate the interface capabilities between the Vericode Symbol/System and the Rockwell automated Information Management System (IMS). Authorization to perform software changes required to support this activity was withheld pending completion of this initial test series.

3.0 APPROACH

The Verisystem evaluation was conducted in four phases as defined by document SSD92-M-0015, NASA MSFC/Rockwell SSD Vericode System Evaluation Plan. The phases were structured to:

- Evaluate the hardware/software and marking equipment used to produce the Vericode Symbol labels

- Generate stencils using photo-process methods

- Mark Space Shuttle Program hardware items made of varying materials and exhibiting a wide range of surface reflectivities/topographies.

- Decode (read) markings under a variety of environmental conditions

The Verisystem was evaluated under conditions normally encountered in the various shuttle manufacturing, final assembly, test, and launch site facilities. The evaluations were accomplished using shuttle orbiter aft fuselage (serial number 098) as the system test bed.

In those cases where actual working conditions could not be duplicated in the test bed environment, they were simulated in the Rockwell Compressed Symbology Testing (CST) Laboratory at 555 Discovery Drive, Huntsville, Alabama 35806.

All marking operations conducted during the evaluation conformed to the requirements of MIL-STD-130, Identification Marking of United States Military Property; Rockwell International Systems Design & Parts (SD&P) publication number 543-G-26, Identification and Marking Requirements; Rockwell International Material Processing Specification (MPS) MA0104-301, Applied Markings; and Rockwell International, Huntsville Operations procedure A-8.1, Identification and Control of MPTA Hardware Removed from OV-098.

4.0 VERICODE SYMBOL DESCRIPTION

The Vericode Symbol is designed to produce extremely space efficient, high data density, machine readable, two-dimensional symbols for use in automatic identification and data entry systems. The Vericode Symbol design is intended to correct deficiencies which limit the use of current linear bar code symbologies. The primary strength of the Vericode Symbol is its ability to be permanently applied directly onto the surface of a wide range of product sizes for subsequent machine capture and decoding.

The Vericode Symbol (Figure 1) includes a rectilinear array of data cells surrounded by one or more orientation borders. The code structure provides high data density, wide substrata versatility, and greater area for detection when using charged coupled device (CCD) detector technology.

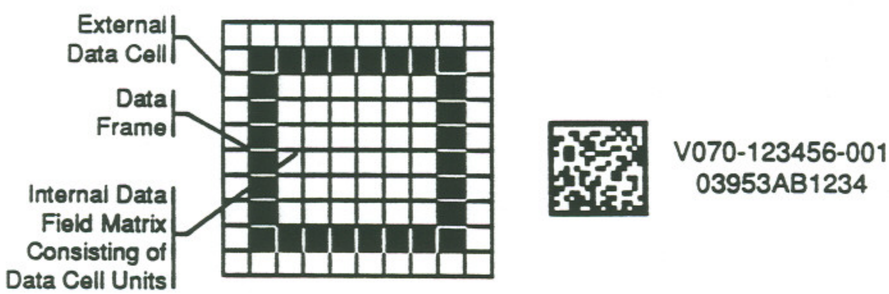

Figure 1. Vericode Symbol structure and example of symbol containing Rockwell part identification data.

The components of the Vericode Symbol are:

- Data cells within the matrix symbol which usually contain a binary bit of information.

- An internal data field comprised of a multitude of data cells

- A data frame, surrounding the internal data field, typically formed from "on" data cells and used for orientation or timing.

- An external data field consisting of data cells which surround the border. This field provides additional information on orientation, timing or symbol identification.

- A quiet zone that surrounds the external data field. This zone is equivalent to one or more concentric rectilinear rings of typically "off" data cells surrounding the outermost pattern of "on" cells. The required number depends on the environment.

The complete Verisystem consists of a software package that can be loaded into a wide range of IBM compatible computers; output devices designed to produce labels or automatically mark hardware items; and decoding devices designed for use with robotic units, in assembly line operations, or work environments requiring portability. Figure 2 illustrates a typical Verisystem input/output operation.

5.0 HARDWARE/SOFTWARE ACQUISITION

The Vericode Symbol generation, marking, and decoding equipment items tested were supplied by Veritec Incorporated, 21821 Plummer Street, Chatsworth, California 91311.

Rockwell International SSD, Huntsville Operations, was responsible for the acquisition and maintenance of equipment used during the system evaluation. All items procured were inspected for identity and damage and tagged as government furnished equipment immediately upon receipt. Accountability of the hardware/software items will be transferred to the NASA, Marshall Space Flight Center, Alabama at the conclusion of Verisystem testing. The Verisystem hardware/software items evaluated are identified in Appendix A.

5.1 Station set-up

After receiving inspection, all Verisystem hardware/software was delivered to the Rockwell CST laboratory where the beta station was set up (Figures 3 through 5). All hookups were accomplished in accordance with supplier instructions.

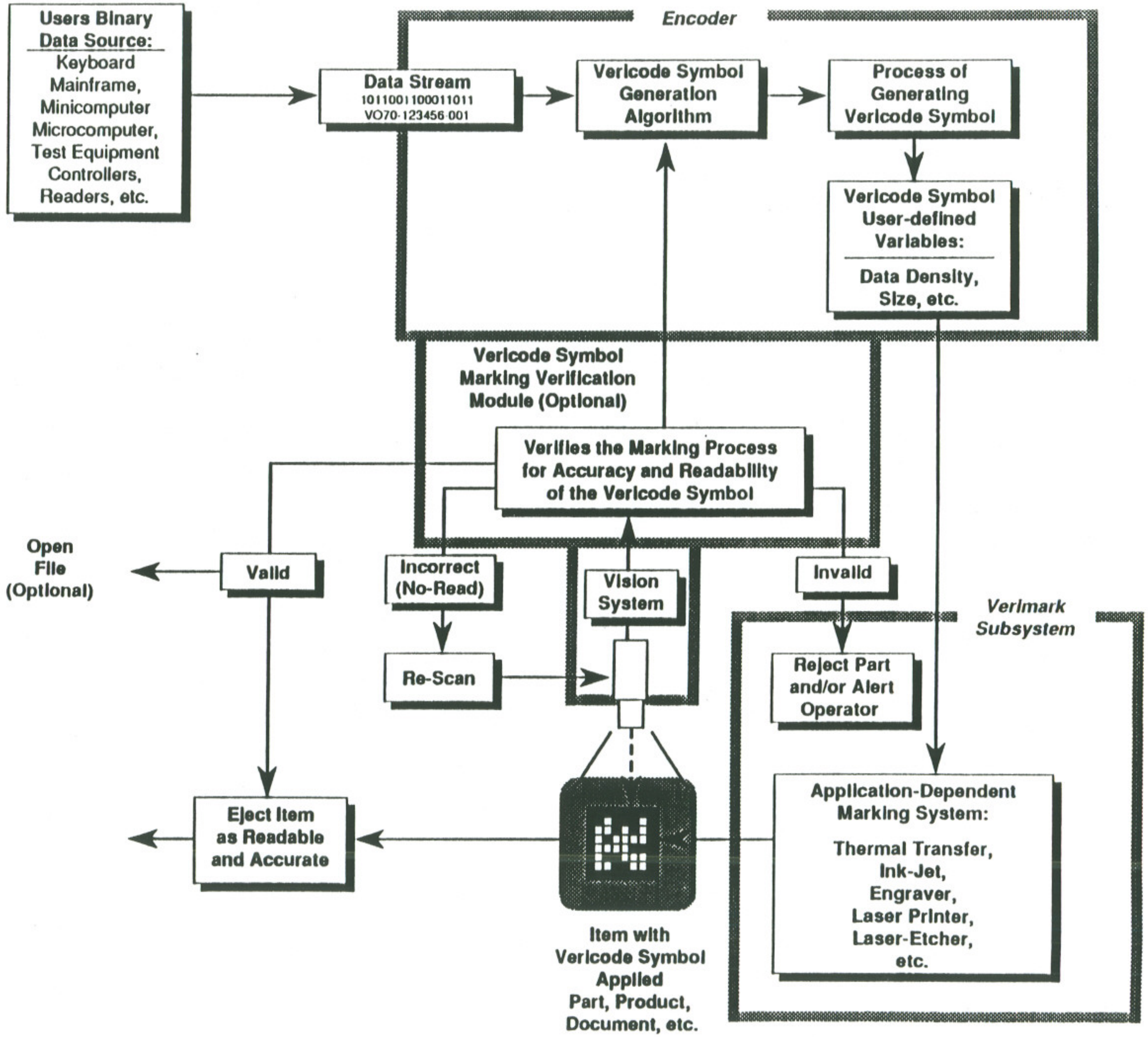

Figure 2. Verisystem Operations Flow

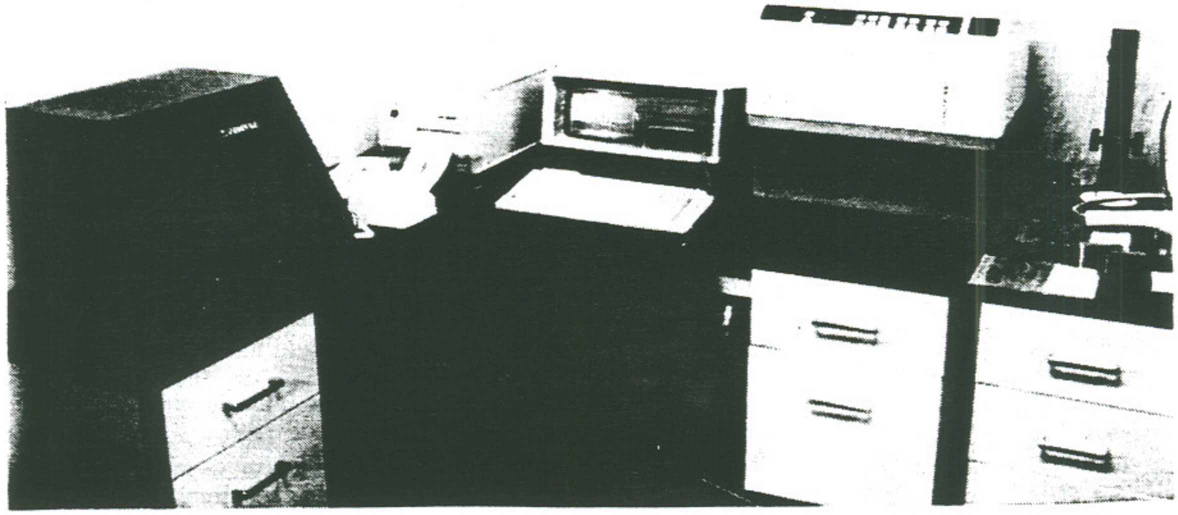

Figure 3. Vericode Symbol label and stencil generation work station.

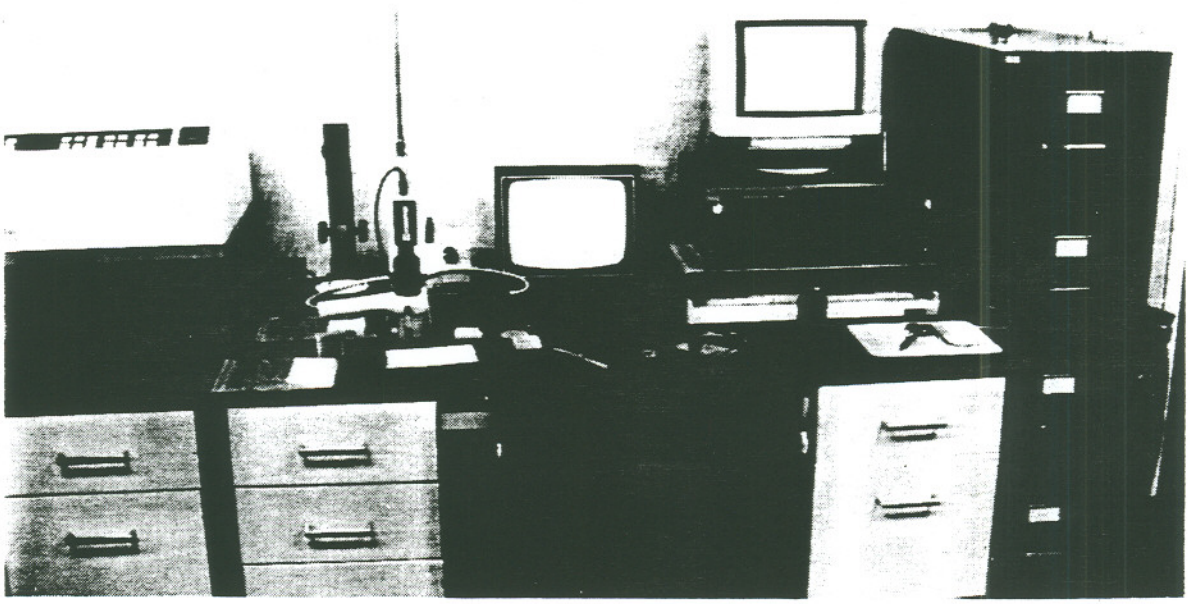

Figure 4. Verisystem fixed scanner decoding work station.

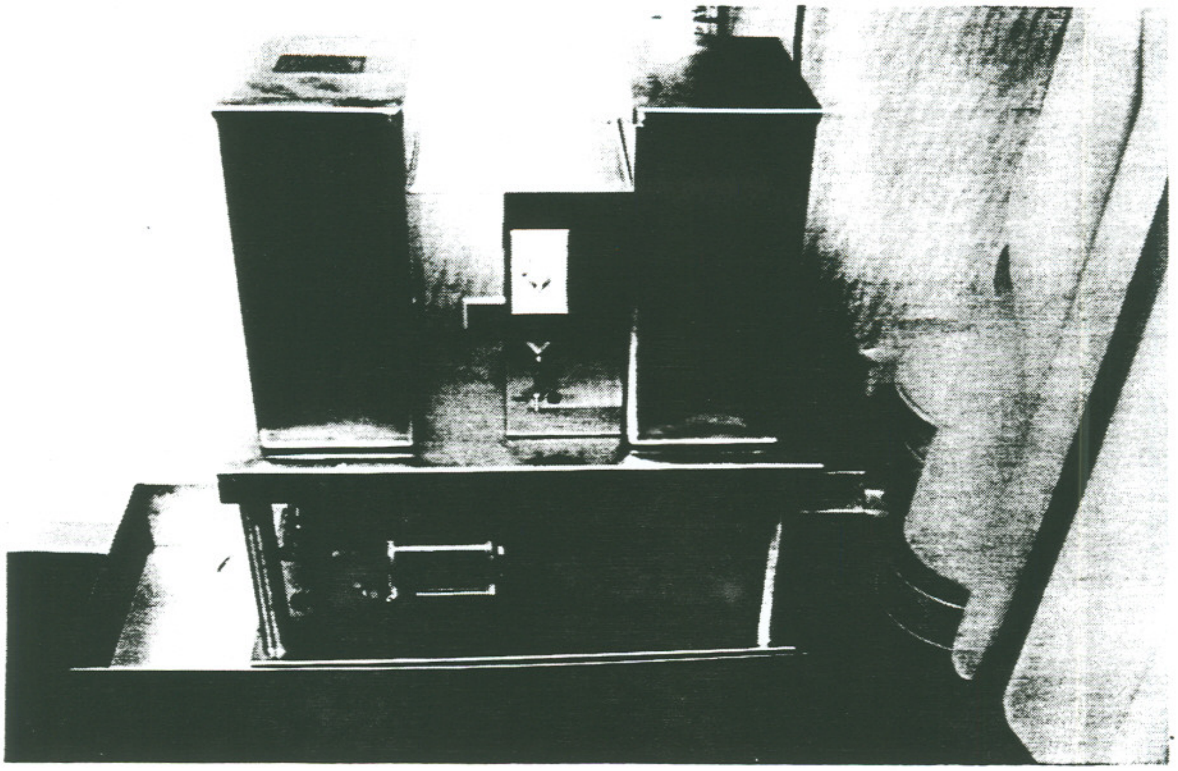

Figure 5. Vericode Symbol stencil developing unit.

5.2 Hazard identification

A formal hazard analysis was conducted May 1-17, 1991 to identify any potential hazards associated with the Verisystem. The results are recorded in document SSD92-M-0016, Huntsville Operations Vericode Evaluation Program Hazard Analysis, and are summarized as follows:

The hazards associated with the Vericode Symbol system hardware items tested were limited to the chemicals used in the electro-chemical etch process. The chemicals are:

5.2.1. Developing fluid

Electro-Chem Etch Metal Markings, Inc. product number PSY-10 is rated as a moderate fire, explosion, and health hazard.

5.2.2. Electrolytes

Electro-Chem Etch Metal Markings, Inc. product numbers SCE-1, SCE-3, SCE-4, SCE-12, and HFE are rated as health hazards.

5.2.3. Cleaner

Electro-Chem Etch Metal Markings, Inc. product number AMC is rated as a health hazard.

5.3 Hazard controls

The methods used by Rockwell to control the hazards identified during the hazard analysis are defined in document SSD92-M-0016 (referenced previously). In addition, the following safety equipment items were required to support the Verisystem evaluation:

- Ventilation system (vent hood and exhaust fan)
- Safety goggles
- Rubber gloves
- Rubber aprons
- OSHA approved eye wash
- Combustible fluid storage cabinet
- Hazardous waste disposal can and liners
- Stainless steel spill containment pan (installed under stencil developing unit)
- Splash shield (used to cover the stencil developing/drying unit electric pump)
- Absorbent spill material
- Electrical surge suppressors
- NFPA Class B/C fire extinguisher

5.4 Equipment burn-in and hardware tests

All Verisystem equipment items used in the beta test station were powered up and run continuously for 48 hours. After the burn-in period each device was tested individually and with the complete system. Two hardware failures and several design deficiencies were noted during the burn-in period. None of the problems were associated with Verisystem production hardware and were subsequently resolved.

Phase 1

Label Generation Tests

6.0 PHASE 1 - LABEL GENERATION TESTS

The primary objective of this test phase was to determine if the Verisystem provides the capability to quickly produce accurate Vericode Symbol labels in the various label sizes currently required by Rockwell drawings/specifications, i.e., 1/16 (.062) to 1 (1.00) inch.

6.1 Label generation process

Vericode Symbol labels are produced by inputting label information and parameters into a computer terminal loaded with the Vericode Symbol generation software. The software converts the incoming data into binary bits (black = "1," white = "0"); formats the bits to a specific character set (ASCII, etc.); assigns the proper location within the Vericode Symbol's data field (matrix); and adds parity checking or other features specified by the user. The information required by the software is contingent upon the marking application. The computer stores the information from the last data entry so the number of data entries is limited after initial input. If requested, an automatic serialization feature will independently advance the serial number by one each time a code is produced.

After the required information is entered, the computer formats the data into code and produces the Vericode Symbol marking by activating the selected output device.

6.2 Label generation tests

A DHprint Cypher IV thermal printer was used during the label generation tests. The printer was programmed to produce Vericode symbols with the corresponding human readable information. This was accomplished to allow for a comparison between the information input into the computer and the output information printed on the label.

During this test series, labels were produced in each of Rockwell's 13 standard marking sizes. The number of characters used in each size grouping ranged from one to a maximum of 72. A total of 500 labels was produced using the demonstration system Vericode Symbol generation software. Each label was reviewed for accuracy, inspected for legibility, and measured and compared against the size requested during the initial input. The results were then charted to bracket the limits of the system.

6.3 Label generation test summary

Standard typing skills are the only requirements needed for production of Vericode Symbol labels. The time required to train an input operator in the fundamentals of the Verisystem label generation process is approximately 10 minutes. Testing verified that information input into the Vericode Symbol generation software was quickly and accurately translated into the Vericode Symbol. The time required to produce a finished label was directly related to the amount of information required to be coded.

Vericode Symbol labels containing a limited number of characters averaged only two minutes to produce. The time required to produce more complicated labels was directly related to the amount of time required to input the additional label information. The times are generally consistent with the times required to produce existing human readable labels.

The smallest readable label that can be produced using 27 characters, a 15 digit Rockwell part number followed by a space and an 11 digit serial number, is 1/8 (.125) inch square. For parts requiring a smaller label, Rockwell could use the six digit order control number (OCN) that is used to relate hardware items to their computer stored historical records. Using the OCN, the label size produced on the DHprint Cypher printer could be reduced to 5/64 (.078) inch square.

It was determined during initial testing that the Vericode Symbol generation (demonstration) software contained label sizing deficiencies. The deficiencies become apparent when producing labels in the smaller size range, i.e., below 1/4 (.250) inch. In this size range the label size produced was directly proportional to the amount of information translated into the Vericode Symbol, i.e., the label size increased as the amount of information increased regardless of the size selected. This problem was discussed with Veritec, Inc. who explained that the demonstration software package was designed to square symbols off to preset sizes, e.g., 1/8 (.125) inch, 1/4 (.250) inch, etc. Subsequent software revisions will provide the capability to produce Vericode Symbols in the desired sizes selected.

Phase 2

Stencil Generation Tests

7.0 **PHASE 2 - STENCIL GENERATION TESTS**

Stencils are used to apply ink, paint, and electro-chemical etch markings to space shuttle hardware. The stencils, currently human readable, are produced using die impression machines, i.e., a typewriter or stencil punch machine. The production of compressed symbology markings requires the use of different stencil generation equipment.

Two new photo-process stencil types were tested during this test series to apply Vericode Symbol markings. The first stencil type was designed specifically for use in the electro-chemical etch marking process. The second was developed for use in micro-sandblasting operations.

7.1 Electro-chemical etch stencil generation procedure

The first step in the electro-chemical etch stencil generation process is to make a transparency (vugraph) from the Vericode Symbol paper label. This is accomplished using any letter quality reproduction machine capable of copying onto vugraph transparency material. The label transparency is then placed (image side down) over an unexposed piece of electro-chemical etch stencil film and exposed to ultraviolet light. The exposed film is developed by saturating it in developing fluid for a prescribed period. The film is then dried using a heat source and stored for later use. The finished stencil is used in the electro-chemical etch process in the same manner that die impression stencils are used.

The equipment used to produce the electro-chemical etch stencil consisted of the following:

- Reproduction machine - Xerox Corporation, model 1065
- Exposure unit - Veritec Inc., Electro-chemical etch stencil exposure unit, model UV-1
- Developing unit - Veritec Inc., supplied Stencil developing and drying unit (prototype)
- Developing fluid - Veritec Inc., supplied PSY-10 developing fluid
- Lighting - Special lighting (yellow bug light) used when working with undeveloped stencil film

7.2 Electro-chemical etch stencil generation tests

Tests were performed to establish the optimum stencil exposure and development times required to produce high quality stencils. With this accomplished, stencils were produced to establish average production times. Care was taken to include a sample from each of the 13 size groupings and to include a mix of character densities. The completed stencils were attached to a standard data sheet where the stencil generation parameters were recorded for use in future marking and decoding tests.

7.3 Electro-chemical etch stencil generation test summary

Vericode Symbol electro-chemical etch stencil production is a simple, straightforward, and uncomplicated process. The time required to produce Vericode Symbol stencils was found to be dependent upon the number of stencils produced in one production cycle. A single stencil, for example, averages 13 minutes to produce, including the time required to make the paper label. When the number of stencils to be produced is increased to 20, the total production time is reduced to an average of 1.6 minutes per stencil.

Production times are broken down as follows:

Stencil generation functions	Time for 1 label	Time for 20 labels
Generate paper label	1 minute	20 minutes
Reproduce label onto transparency (vugraph)	1 minute	1 minute
Expose film (includes four minutes actual exposure time)	5 minutes	5 minutes
Develop film	3 minutes	3 minutes
Dry film	3 minutes	3 minutes
Total time	13 minutes	32 minutes or 1.6 minutes per label

The illustrated time savings are obtainable because the Vericode Symbol exposure, developing, and drying units are designed to accommodate large numbers of stencils per stencil production cycle. The number of stencils that can be produced at one time is only limited by the number of stencils that can fit onto a single stencil film sheet. The stencil film sheets used during this evaluation measured 6-1/2 inches by 13 inches (84.5 square inches). Using this size sheet an operator can easily produce 65 - 70 one-fourth (.250) inch stencils per stencil production cycle. Using 70 stencils as the upper limit, the best production that can be obtained per stencil is 1.17 minutes, or about the same time required to produce human readable labels.

Testing established that the key element in the production of quality stencils is the generation of clear transparencies that exhibit both good definition and contrast. Flaws injected into the transparency from the exposure, developing, or reproduction processes are carried through onto the stencil and hardware marking.

The optimum exposure and developing times required to produce Vericode Symbol electro-chemical etch stencils were determined to be four minutes and two minutes, respectively.

Attempts to use the electro-chemical etch stencil to apply markings using permanent ink or paint proved unsatisfactory.

The only difficulty encountered during this test series was with the accumulation of developing fluid fumes in the laboratory. This problem was corrected by draping a plastic curtain between the overhead vent hood and the prototype developing unit. This removed the developing fluid fumes by directing them into the overhead exhaust fan. Using this configuration, the exhaust fan was only required during developing and drying operations. Production units should incorporate design features to eliminate this problem.

7.4 Micro-sandblast generation tests

The micro-sandblast stencil, like the electro-chemical etch stencil, is produced using a photo-process. The stencils used during this evaluation were obtained through the manufacturer, and the stencil generation process was not tested.

The micro-sandblast stencils are prepared with an adhesive backing so they can be adhered directly to the surface to be marked. To apply the stencil it is heated to a temperature of approximately 100 to 110 degrees Fahrenheit underneath an infrared light bulb for 30 seconds. After heating, the backing sheet is removed and the stencil burnished directly onto the surface to be marked. After marking, the stencil is removed by peeling or by washing with hot soapy water.

Testing established that the micro-sandblast stencils, with some modification (adhesive change), can be successfully used to apply Vericode Symbol markings using the electro-chemical etch, permanent ink, and paint markings methods.

Phase 3

Hardware Marking Tests

8.0 PHASE 3 - HARDWARE MARKING TESTS

The purpose of this phase of testing was to determine if Vericode Symbol markings could be applied to all the various material types and topographies used on the space shuttle program. The effort included an evaluation of Rockwell SSD marking requirements as they relate to the application of compressed symbology markings onto hardware items.

8.1 Rockwell marking procedure

Rockwell identification and marking requirements for spacecraft, spacecraft systems or accessories, and ground support equipment, conform to MIL-STD-130, Identification Marking of U. S. Military Property, and are defined in publication 543-G-26, SD&P Identification and Marking Requirements Manual. Publication 543-G-26 defines the requirements for the application of human readable markings only and does not currently address compressed symbology markings.

8.2 Rockwell marking methods

The marking methods approved for use by Rockwell SSD and the corresponding Standard Design Practices (SDPs) are:

- Case, forged, and molded markings	SDP 174-0008MP
- Electro-arc etch	SDP 174-0003MP
- Electro-chemical etch	SDP 174-0003MP
- Engraved marking	SDP 174-0002MP
- Hot stamp marking	SDP 174-0006MP
- Impression stamp marking	SDP 174-0004MP
- Rubber stamp marking	SDP 174-0007MP
- Stencil marking (paint or ink)	SDP 174-0005MP
- Silk screen marking	SDP 174-0001MP

8.3 Marking tests

The hardware marking tests were conducted in three phases designed to (1) establish the upper and lower size limits for Vericode Symbols when applied to hardware using the electro-chemical etch process; (2) test the Veritec Inc. portable electro-chemical etch kit under field conditions; and (3) to mark parts of different material types, surface contours, textures, and finishes.

8.3.1 Electro-chemical etch size and data density limits

During this test series 66 Vericode Symbol markings were applied to a single sheet of aircraft aluminum using the electro-chemical etch process.

The markings were made in a variety of sizes and data densities. Each marking was examined under magnification (10 power) and the quality of the marking graded. The results of the tests are summarized in Figure 6.

Vericode Symbols were also applied to all the other major metal types and alloys using the electro-chemical etch marking method. The markings were applied using existing Rockwell, SSD and Rocketdyne Division procedures and produced fair to good results.

The markings were made using power, pulse, and time settings to produce a shallow etch resulting in a minimal disturbance of metal surface (approximately 0.0002 inch deep). The electrolytes selected for use produced dark markings, i.e., shades of black, blue, or purple.

Testing established that the size of the Vericode Symbol that can be legibly applied to the metal surface using the electro-chemical etch process is contingent upon the quality of the stencil and the number of characters incorporated into the code. The smallest size Vericode Symbol that can be consistently applied to metal surfaces, using from one to 19 characters of data, is 3/8 (.375) inch square. To apply Vericode Symbols to metal parts in sizes smaller than 3/8 (.375) inch square requires a reduction in the data density, the identification of a higher resolution stencil material, or a switch to an alternative marking method.

8.3.2 Electro-chemical etch field marking

Testing personnel evaluated the Veritec Inc. portable electro-chemical etch marking kit under actual field site conditions. This was accomplished by dispatching inspectors to remote locations to identify parts on a fast turnaround basis. Parts were marked in the following areas:

- Outdoor storage yard and barge dock during various weather conditions

- Difficult-to-reach interior and exterior OV-098 aft fuselage locations

- Receiving inspection dock, material review crib, stock room, and packaging/shipment area

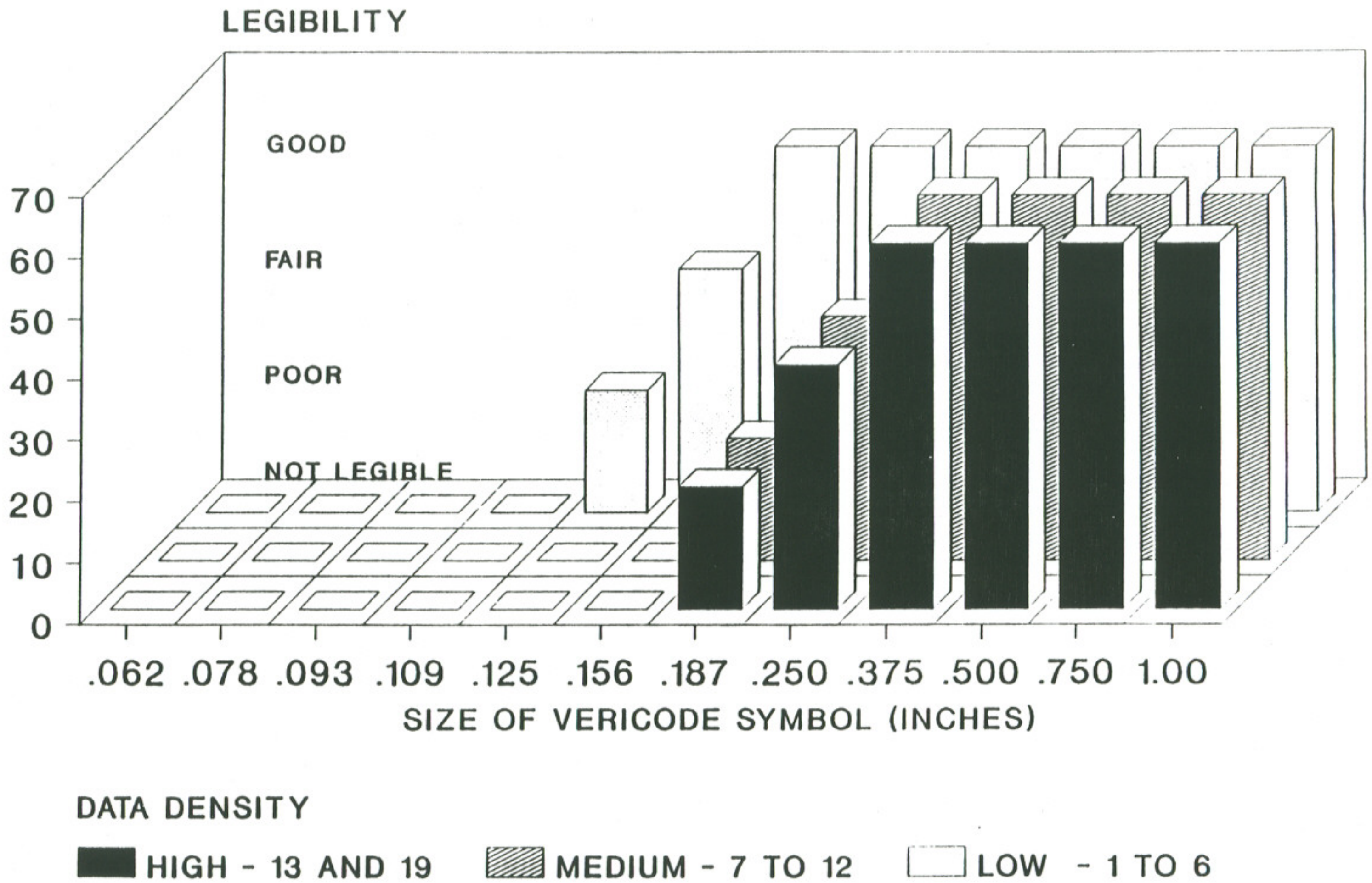

FIGURE 6 **VERICODE SYMBOL CHEM-ETCH TEST RESULTS**
SIZE AND DATA DENSITY LIMITS

The portable electro-chemical etch kit operated successfully under all conditions noted. The only difficulty encountered involved the storage of accessories in the carrying case. The accessories, consisting of various sized applicators, marking pads, cables, etc., were arranged on open shelves within the carrying case. These items were shaken during transportation and in a state of disarray upon arrival at each new work site. This condition was corrected by purchasing a set of seven plastic containers (measuring 1-1/2 inches deep x 3-1/2 inches wide x 6 inches long) with sealing lids to house loose items during transportation. The kit was also supplemented with extra fuses, eye protection goggles, sand paper, isopropyl alcohol, deionized water, lubricating oil, and additional types of electrolytes needed to support Rockwell marking requirements (Figure 7).

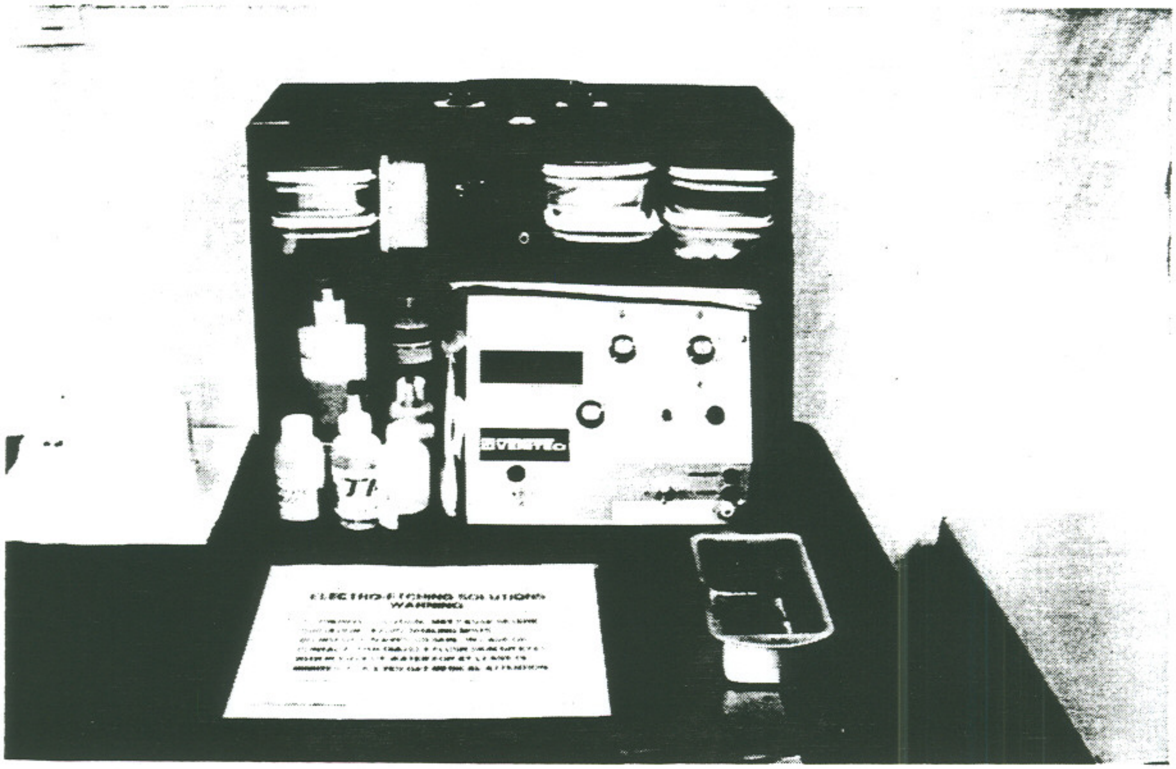

Figure 7. Verisystem portable electro-chemical etch kit.

8.3.3 Material marking tests using Rockwell approved methods

During this test series an attempt was made to apply Vericode Symbol markings onto a sample of each major material type used in the manufacture of the shuttle.

Testing established that all the current Rockwell marking methods can be adapted for use in applying Vericode Symbol markings. The marking methods, however, except for the automated engraving processes, were determined to be generally inadequate for use with compressed symbology systems. The methods can only be used cost effectively if Vericode Symbols are restricted to large sizes, data densities are kept low, and the information coded into the symbol remains constant (lot or member numbers only).

Because of these findings, an evaluation was conducted to identify alternative marking methods that would complement the strengths of the Verisystem. This effort resulted in the identification of several marking methods deemed suitable for the application of Vericode Symbol markings.

8.3.4 Alternative marking method screening criteria

Each of the alternative marking methods identified were jointly screened by Rockwell and Veritec, Inc. to determine their suitability for use on the Space Shuttle Program. This evaluation was performed to eliminate candidates that cannot conform to the following criteria:

- The marking shall withstand all environmental conditions to which the marking is exposed during normal usage.
- The marking shall remain legible throughout the normal life of the equipment used, i.e., 10 years or 100 missions.
- The presence of the marking, or method of marking, shall not be detrimental to the functional performance, reliability, or durability of the item marked, or associated items.

8.3.5 Proposed alternative marking methods

The alternative methods selected for testing were used to mark sample materials, which were evaluated under magnification and retained for future testing. The methods selected and their proposed applications are recorded on Table 1 and described as follows:

Table 1. Proposed Vericode Symbol marking methods

Material Type	Proposed Vericode Symbol Marking Methods													
	*Dot matrix printer	Dot Peen	*Electro chem etch	Engraving	Fabric embroidery	Laser etch	* Laser printer	Micro sandblasting	*Stencil ink	*Stencil paint	* Thermal ribbon	* Thermal transfer	Verimark	Veritape
Ceramic & glass				P		T		P	A	A				
Cloth & fabric					P				A1	A1			P	
Composites		T		T		T		T	A				P	
Cork						T			P	P			P	
Foam insulation									P	P			P	
Metals		P	A	P		P2		P	A				P	P
Painted surface				P		P		P	A	A				
Paper	P						P				P	P		
Plastic.		T		P		P		T					P	
Rubber				T		T							T	
Teflon				T		T								
TPS tile				P		A				P				
Wood									P	P				

P = Preferred marking method
A = Alternate marking method
T = Marking application being evaluated
1 = Contingent upon diameter of thread and coarseness of weave
2 = Direct laser marking should be limited to non-critical applications only
* = Approved Rockwell marking method

8.3.5.1 Dot peen

The dot peen marking method of applying Vericode Symbols to metallic parts (Figure 8) is performed by a computer operated device that drives a round-nose tungsten carbide punch. The device marks the part by striking the surface with the punch repeatedly. The highly localized blows deform and stretch the metal surface, which causes a difference in contrast between the struck and unstruck areas of the part. This difference in contrast can generally be read and decoded by the Verisystem. The success of readability is dependent upon the material being marked. Dot peened materials that do not provide adequate contrast for decoding can be altered by backfilling the recessed areas with a contrasting ink or paint.

Because the surface deformation caused by the peening machine is resisted by the metal underneath, the result is a surface layer under residual compression. This condition is highly crack resistant under fatigue conditions because the compressive stresses are subtractive from the applied tensile loads. The dot peen method is ideally suited for applying Vericode Symbol markings onto shafting, crankshafts, gear teeth, and other cyclic-loaded components.

Using the dot peen method, Vericode Symbol markings containing up to 19 characters can be produced in standard and micro size ranges. i.e., 1/8 (.125) inch square to 3/8 (.375) inch square.

Figure 8. Vericode Symbol marking applied to turbine blade using dot peen marking method.

8.3.5.2 Engraving

The computer driven engraving marking method is a machine process that forms Vericode Symbol markings by removing base material from the hardware surface. This is accomplished using a computer guided cutting tool. The method, approved by Rockwell for use on the orbiter program, appears suitable for marking Vericode Symbols onto most metal and non-metal substrates used on the shuttle program, including items with a variety of surface topographies. Using this method Vericode Symbols can be produced in the 1/8 (.125) inch to 3/4 (.75) inch size range. The legibility of the sample markings provided to Rockwell for evaluation was excellent and will withstand all environmental conditions for which the base material is suitable.

8.3.5.3 Fabric embroidery

The fabric embroidery marking method involves the use of a computer driven sewing machine to stitch a representation of the Vericode Symbol onto cloth or fabric materials (Figure 9). The marking technique, which is still under development, is a simple, cost effective method for applying durable markings onto cloth and fabric materials.

The fabric embroidery marking method could be extremely effective for marking thermal protection system (TPS) blankets. Rockwell currently identifies TPS blankets using the ink stamp marking method. The quality of the marking is generally poor due to the coarseness of the fabric and the markings do not hold up well over time. Efforts are now underway to locate heat resistant black thread that can be used in the fabric embroidery marking process.

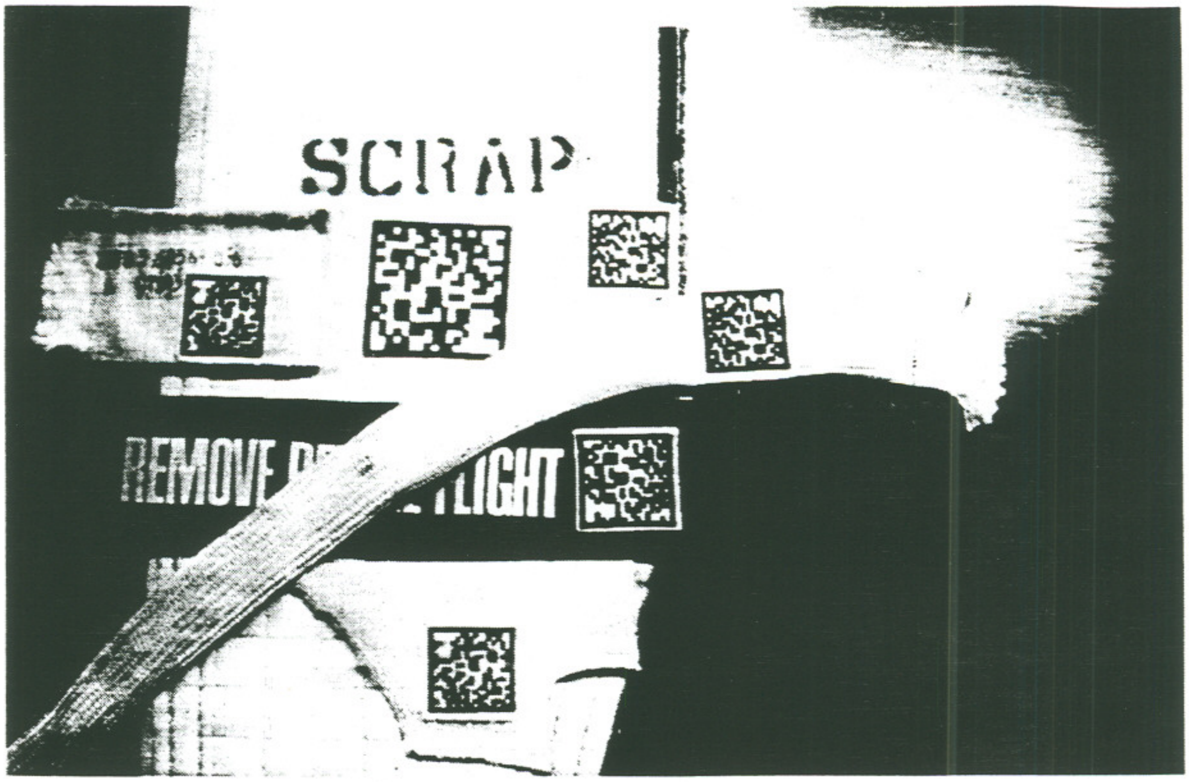

Figure 9. Vericode Symbol marking applied to thermal blankets/ barriers using the fabric embroidery marking method.

8.3.5.4 Laser Etch

The laser etch marking method has been in use since 1976 and has proven to be a highly reliable technology using no inks, foils, chemicals or toxic gases.

New advances in laser design provide the ability to produce quality markings at precise depths by adjusting power and time settings. The adjustments are now so finely tuned that dried paint can be vaporized off a paper surface without discoloring the substrate material.

The computer controlled laser etch method of marking was used to mark a variety of shuttle material types and surface topographies with excellent results. Using the laser etch marking method, readable Vericode Symbols can be produced in the sub-micro size ranges, i.e., smaller then 1/8 (.125) inches square.

Laser etch markings can be applied to hardware using direct or indirect marking methods (labels, metal parts tags, inserts, etc.). The major drawback associated with direct marking in the past was its tendency to alter the crystalline structure of metallic parts through heat transfer. This problem appears to have been minimized in the most current model laser marking devices. Verification testing to conform this will be conducted in the near future. It is unlikely, however, that authorization will be granted to apply direct laser markings onto critical components.

One promising application demonstrated during testing was the marking of orbiter TPS tiles (Figure 10).

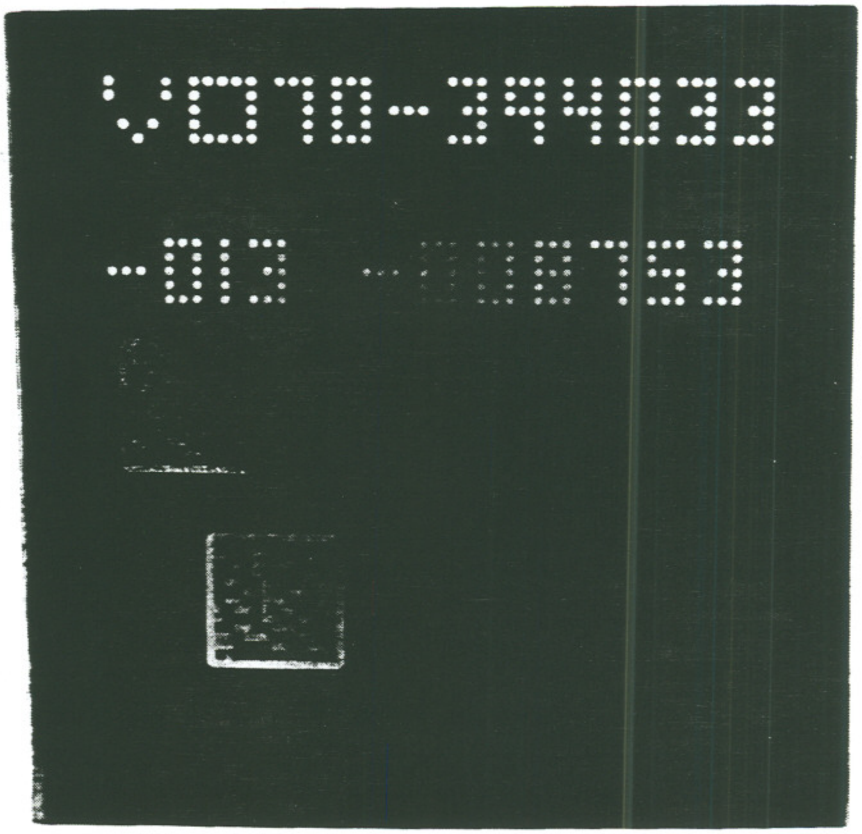

Figure 10. Vericode Symbols applied to TPS tile using laser etch marking method.

The tiles were marked by etching the Vericode Symbol markings into the TPS tile base material to a depth of .004 to .006 inches. The recessed areas were treated with a wetting solution and backfilled with a new high temperature ceramic coating (Verishield) that was sanded flush with the tile surface. The tiles were subjected to heat, hot gas flow, cold soaking, and vacuum testing at MSFC to simulate orbiter flight conditions. None of the tests produced noticeable changes to the Vericode Symbol markings.

Heat and destructive tests performed at KSC produced similar results, i.e., the laser etch process did not affect the substrate and the markings survived conditions that were detrimental to the TPS tile.

Efforts are now underway to obtain NASA approval to fly TPS tiles marked with Vericode Symbol markings on shuttle missions to test the affects of actual environmental conditions.

8.3.5.5 Micro-sandblasting

The micro-sandblasting marking method (Figure 11) involves the use of a computer driven miniature sandblaster that can cut or texture a Vericode Symbol marking onto metallic or non-metallic surfaces.

The micro-sandblasting system operates by directing a mixture of dry air and abrasive through a small tungsten carbide nozzle at high velocity. The software automatically controls the direction of the step-and-repeat table, the length of the stop-and-go pulses, and the speed of flow to produce the requested marking. The system can be accurately adjusted to control the depth of cut.

The micro-sandblasting marking method was used during this evaluation to generate excellent quality markings on windshields and other glass products in sizes as small as 3/8 (.375) inch.

The system contains four parts: the blaster, work station, dust collector, and dry air supply. The abrasive blasting is performed in an enclosed work station to confine the spent abrasive until it can be filtered out by the industrial dust collector.

The air supply must be completely dry so the abrasive does not become moist and plug the nozzle.

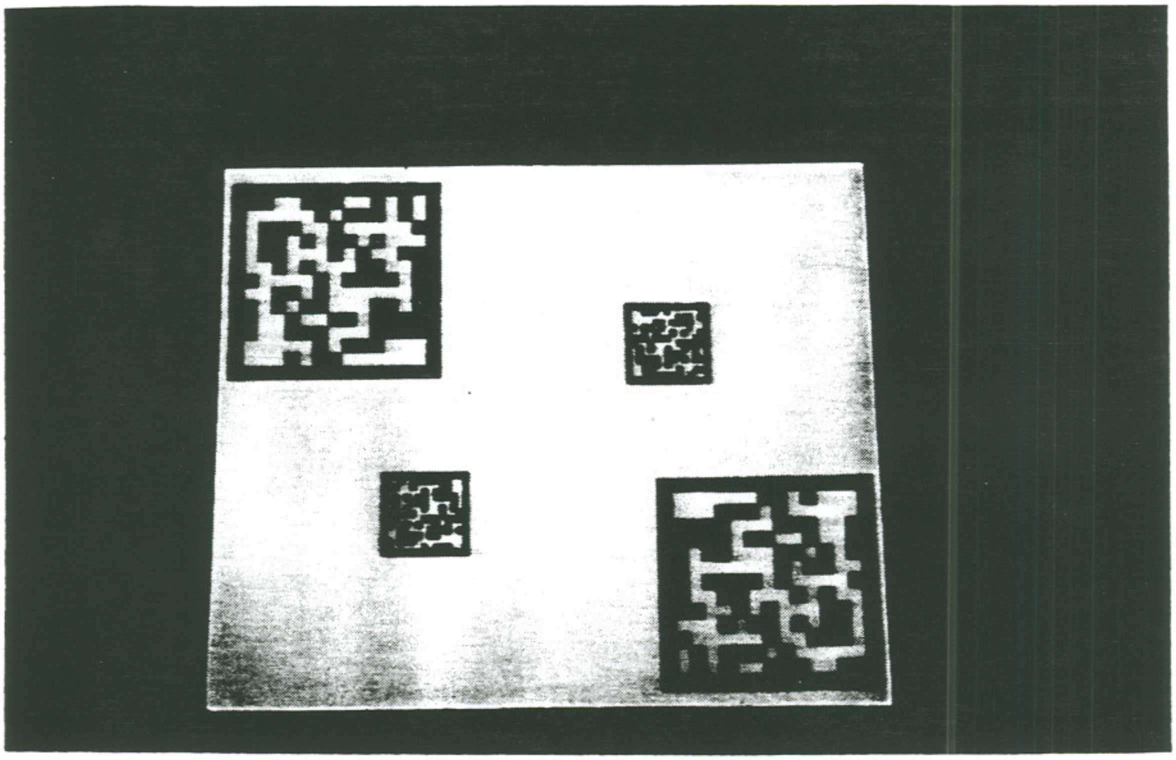

Figure 11. Vericode Symbols applied to metal surface using micro-sandblasting marking method (baking soda used as abrasive).

8.3.5.6 Verimark

The recessed Verimark marking method (Figure 12) involves the marking of Vericode Symbols onto application suitable metallic or non-metallic inserts called Verimarks (patent pending). The Verimarks are coated for environmental protection (if required) and press fit, glued, or screwed into recessed areas drilled or molded into the surface of the hardware item to be marked. The Verimark inserts can be purchased with company logo, program, and project identification applied and color coded to show specific information categories, e.g., part identification, operation and maintenance data, restricted use requirements, and supplemental information (waivers, material review disposition numbers, etc.). Using this method of marking, readable Vericode Symbols can be produced in sizes as small as 1/8 (.125) inch square.

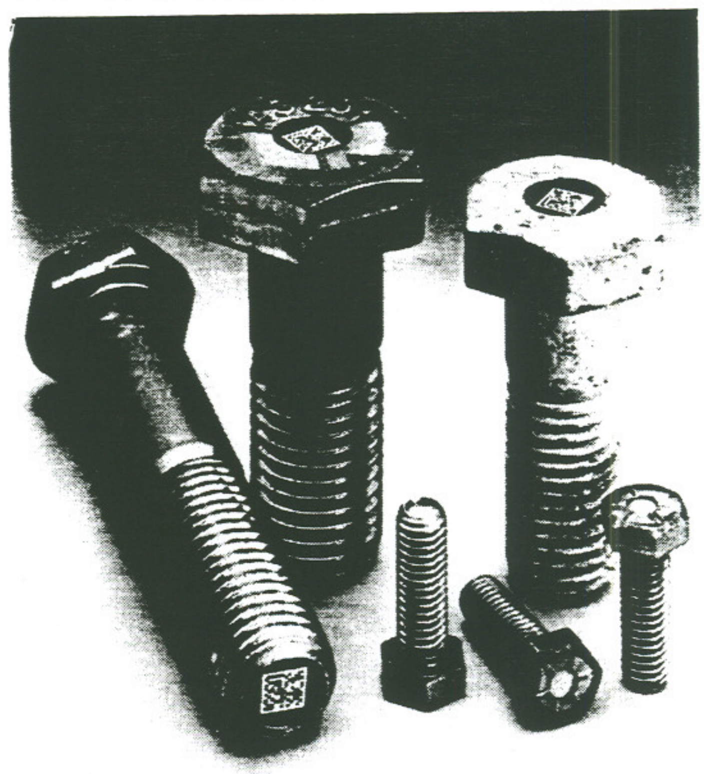

Figure 12. Vericode Symbol markings applied to bolts using Verimark process.

attractive marking options that should be explored as part of follow-on development and testing activities. These include but are not limited to the following:

- Applying Verimarks to buttons or tabs that can be attached to items with difficult-to-mark topographies, i.e., mylar blankets.
- Applying Verimarks to recessed areas of critical bolts, nuts, fasteners, and other metal items which are subject to tool damage.
- Applying Verimarks to recessed areas of items requiring constant handling, e.g., tools, instruments, measuring devices.
- Marking hardware items with rough surfaces which are currently marked using cast, forge or mold methods.

7.3.5.7 Veritape

The Veritape marking method involves the laser etching of Vericode Symbols onto MD172-0027-0001 (MIL-T-9906) pressure sensitive, non-corrosive, heat, cold, and solvent resistant tape per MIL-STD-1247.

The marked tape can then be used to mark lines, pipes, and conduit used in a variety of applications including lines used in hot (above 325 degrees F) or cold (below -60 degrees F) applications. This indirect marking method, like the recessed Verimark, has no detrimental effect on the items being marked. Using this method, Vericode symbols can be produced in the 1/8 (.125) to 3/8 (.375) inch square size range.

Figure 13 illustrates a Veritape marking applied to a four-inch air duct.

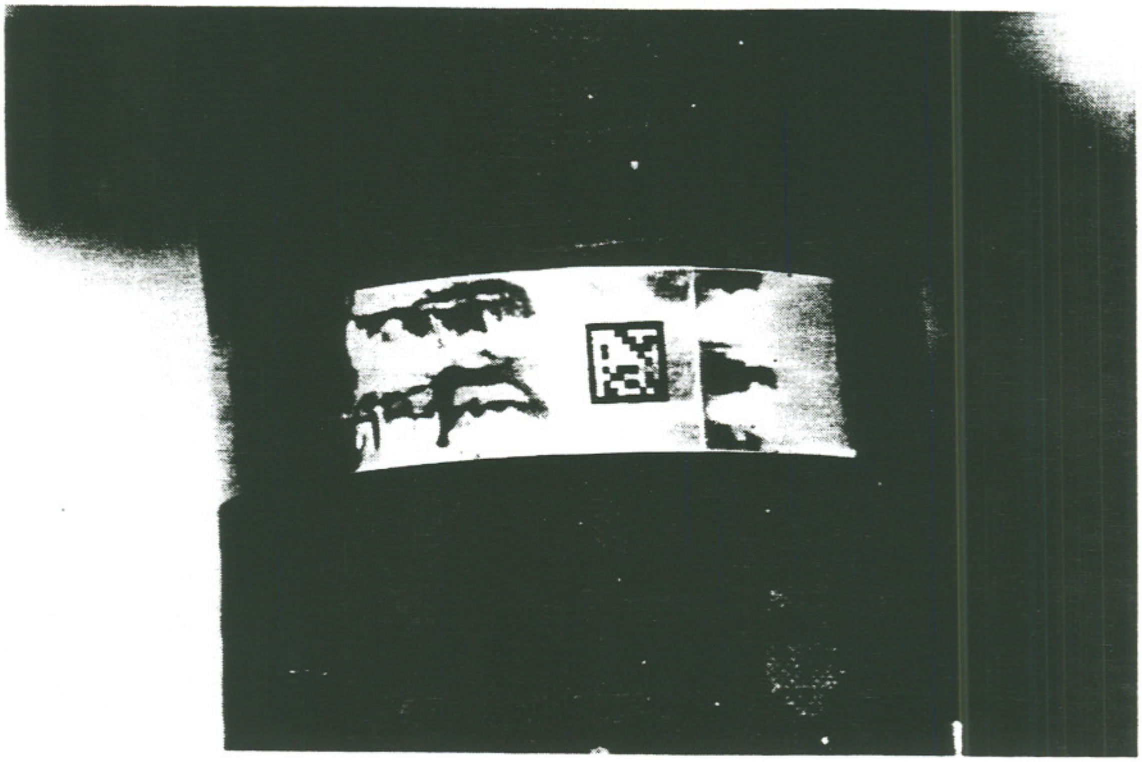

Figure 13. Vericode Symbols applied onto air duct using laser etched pressure sensitive tape

8.3.6 Surface contours, textures and finishes

During this phase of testing Vericode Symbol markings were successfully applied to flat, convex, concave, compound, texture, anodized, painted, pitted, and rough surfaces. The upper and lower limits for these various surface shapes and finishes are defined in Appendix B.

8.4 Hardware marking test summary

Hardware marking tests established that all the major Shuttle material types, surface contours, and surface topographies can be successfully marked with Vericode Symbols, including a large number of hardware items that are too small to mark using conventional marking methods.

The Vericode Symbols can be applied using existing marking methods, modified slightly to accommodate the differences in marking structure, or with several alternative marking methods that provide positive advantages over existing methods.

The testing of these new marking methods was performed in a cursory fashion during this system evaluation and will be expanded during follow-on system development operations. Future efforts will ensure that the marking methods conform to the requirements defined in paragraph 8.3.4. This follow-on effort shall also include cost and tradeoff studies as they relate to marking methods.

9.0 PHASE 4 - DECODING TESTS

The purpose of this test phase was to demonstrate the ability of the Verisystem to read Vericode Symbols under space shuttle processing conditions. The scanning tests were performed using the fixed station scanner and were conducted in the CST Laboratory. The decoding tests were scoped to cover Vericode Symbol scanner distances, data densities, orientation, marking locations, code damage, lighting, surface features, and environmental conditions.

9.1 Decoding test summary

The decoding tests demonstrated that the Verisystem accurately reads Vericode Symbol markings applied to the major shuttle material types under most of the environmental conditions encountered in the workplace. Decoding limits are summarized in Appendix A. Several areas of concern were noted during this test series and are addressed as follows:

Symbol size -

Vericode symbols can be decoded in sizes ranging from microscopic to several feet square. To read these various symbol sizes using the equipment items provided with the Verisystem demonstration package requires that the operator make frequent camera setup adjustments, i.e., change scanner lenses, extension tubes, lens aperture and focus settings, and sometimes, lighting. This process will prove to be both cumbersome and time consuming in an actual shuttle processing environment. Veritec, Inc. is aware of this problem and is developing more flexible decoding devices. The new scanners should include autofocus, zoom lenses, and built-in lighting.

Mobility -

Use of the Verisystem on the space shuttle program will require the availability of compact portable scanners, hardened to withstand the abuses that can be expected in industrial use. Veritec, Inc. is developing a series of portable hand-held scanners to meet these requirements. These devices should be configured as follows:

- Compact wand linked directly to computer terminal via short line (desk/workbench operations).
- Keyboard device with monitor linked to the computer via long line (assembly and test operations).
- Wireless device with over-the-air transmission features (field site operations).

- Wireless device with capture and storage capability - data transferred via hard floppy (off-site operations).

Rockwell is helping this development effort by providing Veritec, Inc. with Rockwell data capture and transfer specifications/requirements and listings of features and functions requiring incorporation into the capture device designs.

Dirt accumulation -

Testing established that, in some instances, dirt accumulation on the last row of the Vericode Symbol markings can result in additional data being added to information coded into the symbol. Veritec, Inc. is currently working on a method to correct this problem.

10.0 FUTURE SYSTEM TEST ACTIVITIES

The Verisystem Evaluation Program was formulated to test the demonstration software package and prototype hardware devices made available to Rockwell/NASA in May 1991. These items are undergoing extensive revision and upgrade and will be tested by Rockwell during follow-on operations. These activities will include the following:

- Perform electro-chemical etch, permanent ink, and paint marking tests using the modified micro-sandblasting stencil.
- Test advanced (unapproved) computer driven compressed symbology marking methods. This effort shall include, but not be limited to, dot peen, machine engraving, fabric embroidery, micro-sandblasting, and high resolution laser etch marking methods.
    - Perform tests to determine if the advanced marking methods noted above degrade the substrate materials they are applied to, e.g., cracks, melting, crystallization, residual stresses.
    - Establish marking size and data density limits
    - Conduct tests to determine the ability of advanced markings to withstand the environmental extremes experienced on the shuttle program.
    - Conduct tradeoff studies related to the selection of advanced marking methods to be used with the Verisystem.
- Test the ability of the system to decode at distance with a telephoto lens.

- Perform Vericode Symbol software damage reconstruction tests
- Test Vericode Symbol capture devices needed to support the various Rockwell receiving, manufacturing, test, and flight operations, i.e., multipurpose fixed scanner, portable linked scanner, and wireless scanner.
- Test Verisystem data transfer device, e.g., wedge box
- Perform interface tests between Verisystem and the various Rockwell inspection and measurement devices.
- Conduct a study to determine the feasibility of using the portable Vericode Symbol scanner to capture and electronically transfer hardware discrepancy images to the appropriate files in the automated problem reporting system.

11.0 PROPOSED SYSTEM APPLICATIONS

Testing has established that the Verisystem is a workable concept. System development has now reached a point where limited application is both practical and desirable. Because the portable handheld scanner and computer interface devices are still under development, initial application should be limited to fixed scanner settings that are operated off-line of the mainframe computer, i.e., controlled via simple (non-integrated) computer programs.

A tool crib would provide an excellent area to begin initial implementation activities because the items to be marked would be consolidated/accessible and the tracking accomplished in a standalone computer system that can be easily modified. The tool crib also provides an environment that allows the system to be tested under actual working conditions without excessive risk or disruption of operations.

Three different tool crib operations are currently in the planning stages and will be tested in the future. The cribs will be operated by the United States Navy Air Depot, Cherry Point, Virginia; Newport News Shipbuilding, Newport News, Virginia; and Martin Marietta Corporation, Michould Assembly Facility, New Orleans, Louisiana. These efforts will be closely monitored and supported by the existing joint Veritec, Rockwell, and NASA/MSFC Verisystem development team. The experience gained in the prototype tool crib control stations could be quickly expanded to include other contractor tool cribs and similar fixed station applications (technical libraries, calibration laboratories, etc.).

To assist the development of the Verisystem for mainstream operations, NASA/MSFC has expressed a need to establish a joint aerospace contractor Verisystem Development Team. Participation in this effort would be voluntary and would involve the acquisition of one or more prototype Vericode work stations. The prototype systems would be purchased by the participating contractors.

Team members would place work stations in a wide range of functional areas where actual hands-on experience could be gained. The stations would be used as a proving ground where assigned project managers could develop specifications and requirements for the system as they apply to their individual functions. The task would include the identification of desired changes to the system that would enhance its usability in the various operations. The specific system specifications and recommended changes would be funnelled through the Huntsville CST laboratory where required software/hardware modifications would be coordinated with the manufacturer, hardware/software changes tested, and reports distributed. This shared development/cost approach would be continued until the system was certified for use.

Rockwell's participation in this effort would be to provide support in several key areas of responsibility, strength, and uniqueness, i.e., system integration, configuration management, and thermal protection system.

12.0 POTENTIAL COST SAVINGS

The cost savings to be derived from the use of the Verisystem is dependent upon the depth of application and is directly proportional to the size of the program and length of operations.

Although a detailed breakdown of savings cannot be presented, some conservative examples can be provided for illustration purposes. Five are listed as follows:

1. The Verisystem software is currently being designed to drive hardware marking devices via computer. The quality of the machine-generated markings evaluated are superior to the markings applied by hand. The machine marking devices, being computerized, can be linked directly to the engineering drawing and production control systems where edit software could verify the accuracy of part identification data prior to being applied to the hardware. This improvement will reduce the number of human errors that could be injected into products, resulting in reduced costs.

2. Operators on the floor are required to mark parts as defined per drawing (usually a specification reference). By modifying the hardware marking device driver software to ask the appropriate questions, the software could select the required marking device and apply the markings as defined by NASA specifications. The automation of the marking process would simplify operations and reduce human errors. Assuming these steps would save approximately five minutes per marking, the net savings for each orbiter manufacturing cycle would be significant.

3. If the newly developed high temperature ceramic coating used during this test program to apply Vericode Symbol markings to TPS tile is certified for flight, substantial savings could be obtained. These savings would be derived through a reduction of time spent researching the identification of tile with faded or lost markings and by eliminating a large number of periodic tile remarking operations. The cost savings gained in this area have not been calculated because of the many variables involved but are expected to be substantial.

4. If the advanced marking systems proposed in this report are adopted for marking fasteners, NASA could eliminate the need to reidentify fasteners each time they are issued to the shop floor or removed from their next assemblies. The markings also would provide verification of proper configuration prior to installation and reduce the risk of counterfeit fasteners being introduced into the products. The tangible cost savings derived from these actions are expected to more than offset the cost of the initial marking operations.

5. Automatic transfer of hardware identification into information management systems would not only reduce the number of hours expended on data input but also would reduce the number of input errors caused during the transfer of information. These errors occur in operations used to transfer information from the drawings to the hardware, from the hardware to the work authorization documents (WADs), and from the WADs to the computer. Elimination of these errors would save thousands of hours of work currently expended on research and correction.

In summary, the Verisystem, if implemented, would be cost effective, streamline NASA/contractor operations, and break down a major barrier to the introduction of a paperless environment . . . the electronic transfer of identification data from the hardware to the computer.

Appendix A

Verisystem Hardware/Software Items Evaluated

Appendix A. Verisystem Hardware/Software Items Evaluated

Hardware/software items evaluated during the Vericode automated Identification System (Verisystem) Evaluation:

Code/decode hardware

- Compac Computer Corporation, Compac Portable II Computer, model 2650 (loan item)
- Veritec Inc., Verisystem Encoder/Decoder (computer), model number E/D 1200
- Javelin Electronics, Inc., black & white CCTV monitor, model number BWM12
- Techni-Quip Corporation, scanner, model number T-Q/V-B
- Techni-Quip Corporation, Charged Coupling Device (CCD), model number T-Q/VBOB
- Unitron, 1-inch tube lens
- Fuji Photo Optical Company, Fujinon TV lens, 1:1.4/50, model number CF50B
- Computar, TV Zoom Lens, 1:1.2/12.5 - 75, part number 105357
- Cosmicar Lens Division, ASAHI Precision Company, LTD., C-mount Extension Tube Set, part number 90100 EX-C6
- Scanner stand
- Techni-Quip Corporation, Illumination System, model number TQ/FOI-1 with fibre optic bifurcated lens and annular ring
- Tiffen 77MM Polarizer/Analyzer Kit
- New Image Video Scanner System, model number 020419 (Veritec Inc. loan item)
- OralCam Video Scanner System (Veritec Inc. loan item)
- Welch Allyn Video Probe, model 2000 (GFE)
- Veritec Inc. prototype Portable Hand-Held Scanner (Veritec, Inc. loan item)

Marking hardware

- RJS, Inc., ThermaBar Printer (ribbon), model number IP-7101
- DH Technology Company, Cypher IV Demand Label Printer (thermal transfer), model number 546
- Veritec Inc., Vericode Symbol Stencil Film Exposure Unit, model UV-1
- Veritec Inc., Vericode Symbol Stencil Developing Unit (prototype)
- Metal Marking, Inc., Electro-chemical Etch Kit, model number 500

Software

- Vericode Symbol Generation (V-gen) demonstration and intermediate development programs
- Vericode Symbol Capture and Decoder (Verivision) demonstration and intermediate development programs
- Vericode Symbol Marking (Verimark) - Limited evaluation - marking equipment not available

Appendix B

Verisystem Specifications

Appendix B. Verisystem Specifications

1. Computer requirements:

Required memory	TBD

2. Power requirements (Microprocessor):

AC Cord	UL approved, 3-pin
Input voltage	110 VAC
Frequency	60 HZ
Power comsumption	+5v @2.4A typical (1MB version) -5V @.0.A* typical (all versions) +12V @0.0A* typical (all versions) -12V @0.0A* typical (all versions) * Available but not used by the 386 as shipped

3. Code generation:

Character set options.	4, 5, 6, 7, and 8 bit
Code size	Output device dependent - generally 1/8 to 3 inches
Code shape	Square or rectangle Destacked code (string) in work
Data Redundancy	No - in work
Data Reconstructability	No - in work
Data Security	No - in work
Maximum number of characters . .	195 characters (output device dependent) generally 5 to 30

4. Suggested marking methods:

Marking systems	Item Number	Lot or member number	Serialized or variable data
Case, forge or mold	Yes		
Dot matrix printer	Yes	Yes	Yes
Dot peen	Yes	Yes	Yes
Electro arc etch	Yes	Yes	Yes
Electro chemical etch	Yes	Yes	
Electro vibration etch	Yes	Yes	Yes
Electron beam writer	Yes	Yes	Yes
Embossing *	Yes	Yes	
Embroidery	Yes	Yes	Yes
Engraving	Yes	Yes	Yes
Flexographic printing *	Yes	Yes	

Gravure Printing - Rotary * .	Yes	Yes	
Gravure Printing - Flat * . .	Yes	Yes	
Hot Stamp *	Yes	Yes	
Impression Stamp *	Yes	Yes	
Ink Jet	Yes	Yes	Yes
Ion Deposition	Yes	Yes	Yes
Label (Paper)	Yes	Yes	Yes
Label (Foil)	Yes	Yes	Yes
Label (Metal)	Yes	Yes	Yes
Laser Etch	Yes	Yes	Yes
Laser Printer	Yes	Yes	Yes
Micro-Sandblasting	Yes	Yes	Yes
Offset Printing *	Yes	Yes	
Photocomposition	Yes	Yes	Yes
Rubber Stamp *	Yes	Yes	
Stencil (Ink and Paint) * . .	Yes	Yes	
Silk Screen *	Yes	Yes	
Thermal Ribbon Printer	Yes	Yes	Yes
Thermal Heat Printer	Yes	Yes	Yes

* = Requires original artwork for each Vericode Symbol

5. Marking Parameters:

Low Data density symbol (one to six characters) applied using Rockwell approved Electro-chemical etch, permanent ink, and paint marking methods.

Surface Shape

Flat surface	Minimum 3/16 (.187) inch
Convex surface	Minimum 1/4 (.250) inch - Optimum size equal to the full length of the radius (57 degree arc)
Concave surface	Minimum 1/4 (.250) inch - Optimum size equal to one half the radius of the curve
Compound surface	Minimum 1/4 (.250) inch - Optimum size is approximately 17 to 18 percent of the diameter of the sphere

Surface Finish

Anodized surface	OK (paint and ink markings only)
Painted surface	OK (paint and ink markings only)
Pitted surfaces	Results fair to poor - difficult to fill voids in surface material
Rough surface	Marking quality drops off when surface roughness exceeds 64 on microfinish comparator. Unacceptable above 125 microinches.

6. Decoding:

Camera-to-Target Distance. . .	2.25 to 13.10 inches - Camera lens dependent - Long distance decoding tests using telephoto lenses in progress
Code Orientation to Scanner (Tilt between X and Y axis). .	80 degrees
Code Orientation to Scanner (Rotation around Z axis) . . .	360 degrees
Code Shape	Square or Rectangle (maximum ratio .03 to 1.0) Destacked code (string) under development
Data Density by Symbol Size . .	Output device dependent - DHprint Cypher IV Thermal Printer shown for illustration purposes: 1-4 characters (.093") 5-9 characters (.125") 10-16 characters (.187") 17-19 characters (.250") 22-62 characters (.375") 63-78 characters (.500") 79-up - Will not decode
Light Requirements	3-2000+ footcandles. Will read under all colors in the visible light spectrum. Software can overcome up to 49% difference in data cell contrast caused by shadows or reflection. Speculate reflection can be controlled using conventional photographic techniques.
Airborne Obstructions	Software can decode under fog, mist, stream, cryogenic vapor, and smoke conditions which do not reduce the light levels by more than 50 percent.
Vibration	Random vibration - 0-2000+ Hz, 1.262 to 10.26+ g's at .10 amplitude Fixed vibration - 5 Hz at .1 amplitude 10 Hz at .07 amplitude 15 Hz at .06 amplitude

Marking Location	Not affected by surface features outside of camera view. Software will tolerate surface feature within camera view if they do not touch the Vericode Symbol marking or fall within the code location scanning area.
Surface Shapes	Vericode Symbol markings can be read from flat surfaces, concave/convex surfaces when the marking does not exceed one-half of the diameter of the curve, and compound surfaces if the marking does not exceed 37 percent of the diameter.
Surface Topographies	Vericode Symbol markings can be read from transparent, translucent, opaque, colored, and shiny surfaces which do not exceed 65 on the microfinish comparator surface roughness scale. The readability of Vericode Symbols applied to fabric surfaces is contingent upon the size of the thread in the fabric, density of weave, size of symbol, and the amount of information in the code. Pitted surfaces can not be read if the marking does not color the voids.
Moisture	Moisture (including salt spray) does not impede the decoding process unless it beads or freezes on the marking surface. The system will decode under submerged conditions when the water is clear and sufficient light is present.
Temperature	Decoding not affected by material expansion/contraction resulting from temperature changes
Chemical Films.	Decoding is not affected by thin films of commonly used aerospace chemicals. Oil and grease products will interfere with the decoding process when applied liberally over markings.

Dirt Accumulation	Dirt accumulations will result in either a valid code, non-read or misread. Misreads occur when dirt accumulates on blank rows of code, excluding corners. A software change is in work to prevent blank row misreads.
Symbol Damage	Software programming to reconstruct damaged Vericode Symbols is under development

7. System operating environment:

Ambient Temperature limits . .	Operating 0 - 40c (32 to 104)F Storage -30 to 70c (-22 to 158)F
Humidity	Up to 80 percent relative humidity, noncondensing
Vibration (Camera)	15g's at 60hz to 1000hz 5g's RMS random vibration without damage
Shock (Camera Less lenses) . .	Up to 15g's in any axis under nonoperating conditions per MIL-E-5400T, paragraph 3.2.24.6, camera head up to 30g's
Altitude	Sea level to equivalent of 3048 meters (10,000 feet) 508mm/20inches of mercury

8. System documentation:

Hardware/Software Description	Yes
Specifications	Yes
Installation	Yes
Operation	Yes
Trouble Shooting	Yes

9. System warranty:

Monitors	TBD
Computer	5 years from date of shipment (Does not include any ROM BIOS provided on board)
Camera/Scanner	TBD
Illumination System	TBD
Marking Devices	Varies with supplier